WHAT IS CLAIMED IS:

1. A method of fabricating a lead frame for a semiconductor device package, the method comprising:

providing a first metal layer;

patterning a mask over the first metal layer to reveal exposed regions;

electroplating a metal over the exposed regions;

removing the mask; and

encapsulating at least a portion of the first metal layer and the electroplated metal within a dielectric material.

2. The method of claim 1 wherein providing the first metal layer comprises providing a copper roll, and electroplating the metal comprises electroplating additional copper.

3. The method of claim 2 further comprising creating a pattern of holes in the first metal layer to define a lead frame comprising a diepad portion separated from a pin portion.

4. The method of claim 3 wherein creating the pattern of holes comprises etching completely through the first metal layer.

5. The method of claim 3 wherein creating the pattern of holes comprises stamping completely through the first metal layer.

6. The method of claim 1 wherein the electroplating forms a QFN package pin portion exposed following encapsulation.

7. The method of claim 6 wherein the electroplating forms a diepad portion exposed following encapsulation..

8. The method of claim 1 wherein electroplating the metal forms a raised feature on an upper side of a diepad of a power-type package selected from the group consisting of TO-247, TO-220, DPAK, D2PAK, SO-x, and power BGA, for ensuring even spreading of adhesive and resulting uniform attitude of a die placed attached to the upper surface.

9. A method of fabricating a lead frame for a semiconductor device package, the method comprising:

providing a first layer;

patterning a first mask over the first layer to reveal first exposed regions;

electroplating a first metal over the first layer in the first exposed regions;

patterning a second mask over the first mask to reveal second exposed regions;

electroplating a second metal over the first mask in the second exposed regions;

removing the first and second masks; and

encapsulating at least a portion of the first metal and the second metal within dielectric material.

10. The method of claim 9 wherein the first metal and the second metal are the same.

11. The method of claim 9 wherein:

patterning the first mask comprises patterning a negative photoresist mask; and

patterning the second mask comprises patterning a negative photoresist mask.

12. The method of claim 11 wherein removing the negative and positive photoresist masks defines a lead frame comprising a diepad portion and a pin portion, the method further comprising:

encapsulating the lead frame within a plastic package body; and

separating the first metal from the first layer, wherein the first exposed regions correspond to a pin portion exposed on a surface of the package body.

13. The method of claim 12 wherein the lead frame is encapsulated within a cell of a mold, such that individual packages are singulated upon separation of the first metal from the first layer.

14. The method of claim 12 further comprising:

forming an etch stop layer over the first metal prior to forming the second metal;

etching a portion of the first metal revealed by separation from the first layer to form a cavity; and

introducing additional dielectric material within the cavity.

15. The method of claim 14 wherein forming the etch stop layer comprises electroplating a metal different from the first and second metals within the first exposed regions.

16. A lead frame for semiconductor device package, the lead frame comprising:

a diepad comprising a metal;

a pin separate from the diepad; and

an electroplated raised feature comprising the metal, formed on at least one of the diepad and the pin.

17. The lead frame of claim 16 wherein the raised feature comprises a QFN package pin portion extending to a surface of the package.

18. The lead frame of claim 17 further comprising a second raised feature comprising a portion of the diepad extending to the package surface.

19. The lead frame of claim 16 wherein the raised feature is located on an upper surface of the diepad for ensuring even spreading of adhesive and resulting uniform attitude of a die placed attached to the upper surface.

20. The lead frame of claim 16 wherein the raised feature comprises a stud on the pin for elevating a power ball grid array (BGA) package above a surface.

21. The lead frame of claim 16 wherein a perimeter of the diepad exhibits a serpentine shape.

22. The lead frame of claim 16 wherein the pin lies between the diepad and an outer pin.

23. The lead frame of claim 22 wherein the raised feature comprises an additional thickness of the outer pin, such that the outer pin is taller than the pin.

24. A method of fabricating a metal lead frame, the method comprising:

patterning a negative photoresist mask over a substrate;

electroplating raised portions of a copper lead frame within regions exposed by the negative photoresist mask;

patterning a positive photoresist mask over the negative photoresist mask and the raised copper portions;

electroplating diepad and pin portions of the copper lead frame within regions exposed by the positive photoresist mask;

removing the negative and positive photoresist masks;

attaching a die to the diepad;

encapsulating the die and lead frame within plastic; and

separating the raised copper portions and the plastic from the substrate.

25. The method of claim 24 further comprising singulating the encapsulated die and lead frame from adjacent packages by sawing.

26. The method of claim 25 wherein:

the die and lead frame are encapsulated within a cell of a surrounding mold; and

separation of the raised copper portions and the plastic from the substrate is accomplished by chemical etching, resulting in singulation of the encapsulated die and lead frame from adjacent packages.

27. A method of fabricating a lead frame for a power ball grid array (BGA) semiconductor device package, the method comprising:

providing a first metal layer including a pin portion;

patterning a mask over the first metal layer to reveal an exposed region on the pin portion;

electroplating a metal over the exposed region to form a raised pin feature; and

removing the mask.

28. The method of claim 27 further comprising:

providing a PC board bearing a solder ball; and

placing the raised pin feature into contact with a PC board, such that a body of the power BGA package is elevated above the PC board in contact with the solder ball and preserving a rounded shape of the solder ball.